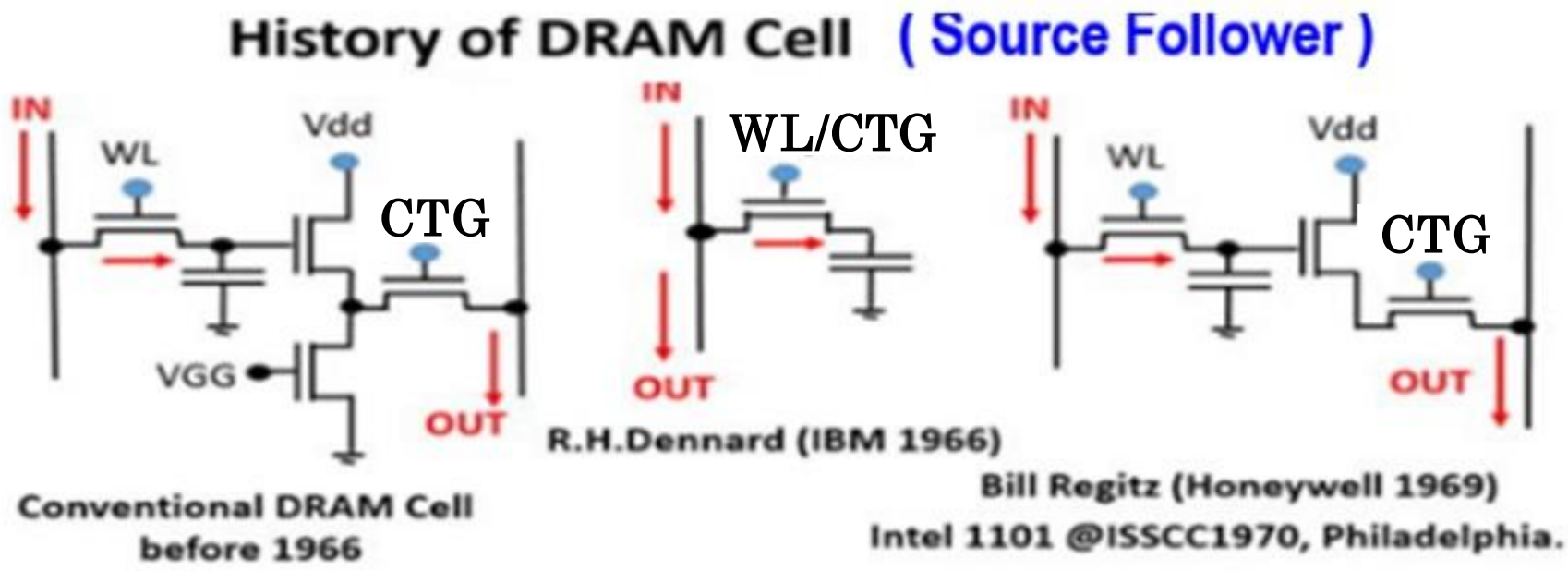
3 1T1C DRAM and Classical MOS type CTD

Under Construction

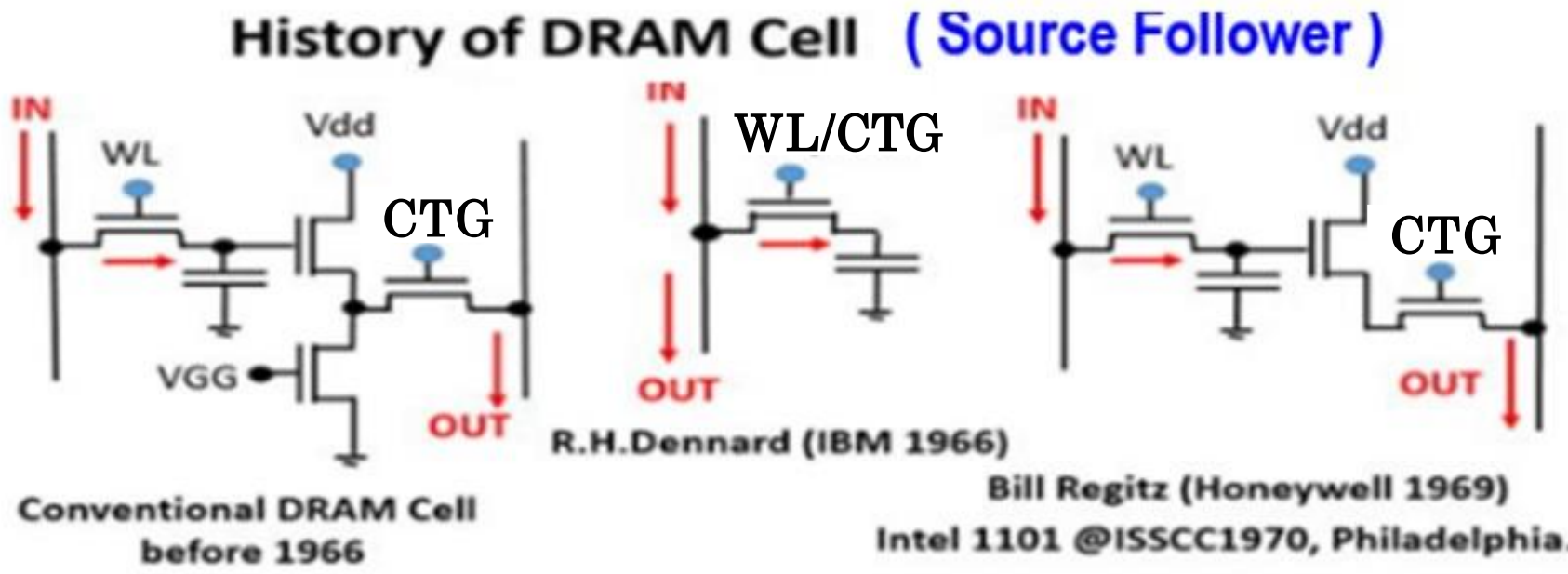
3 1T1C DRAM and Classical MOS type CTD

Around 1966, the first DRAM cell was composed of four MOS transistors and one capacitance (4T1C). The signal charge is stored in the source diffusion capacitance thru the input MOS transistor and is read out by the three output transistors, composed of two transistor source follower current amplifier circuit and one column read out line switch MOS charge transfer gate (VOG).



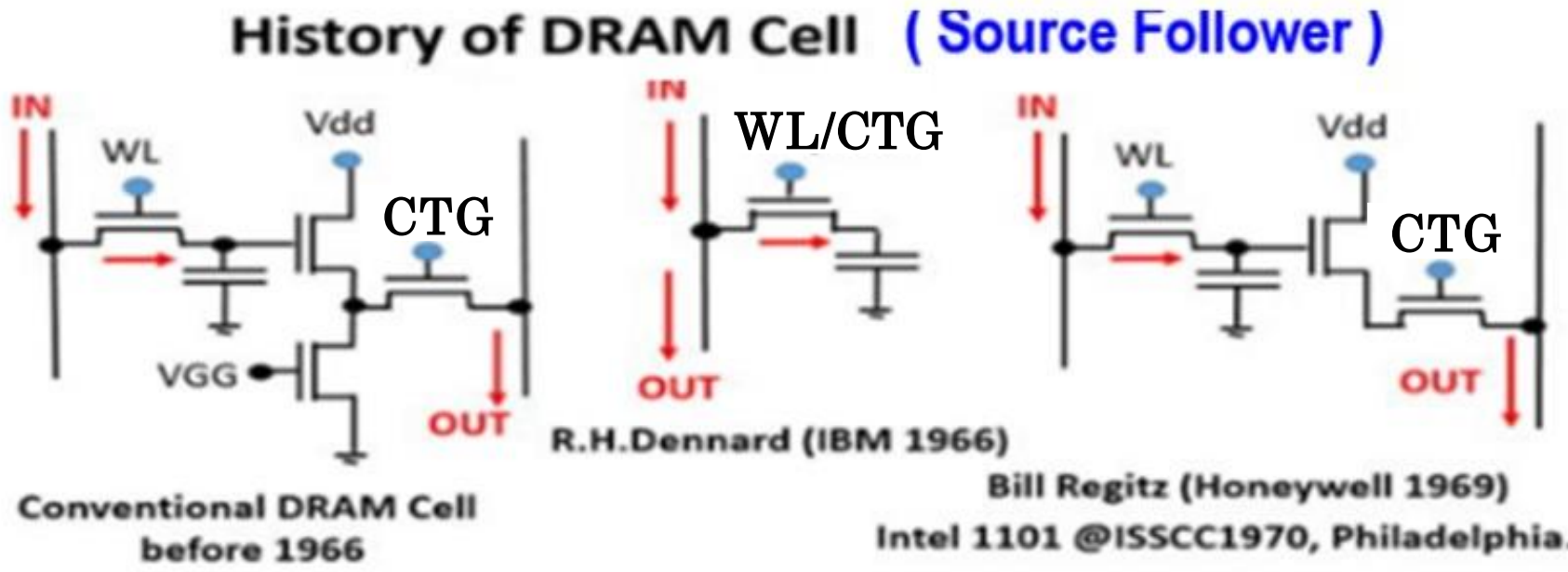
3 1T1C DRAM and Classical MOS type CTD

One Transistor One Capacitor (1T1C) DRAM Cell was then proposed by R.H. Dennard at IBM 1966. Even though the output signal is a digital nature, the output signal amplitude is very small due to the output bit line large capacitor charge distribution effect. It was before the development of the dynamic column sense amplifier circuit which is feasible to mass production.



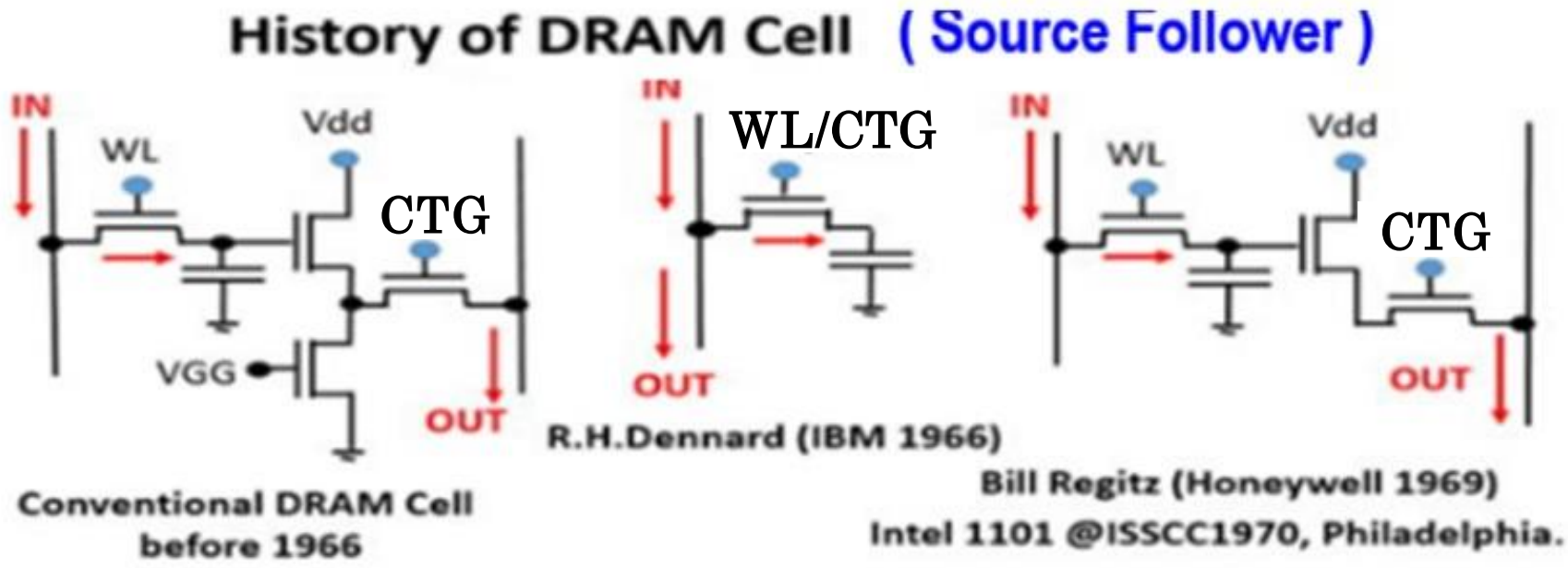
3 1C1T DRAM and Classical MOS type CTD

In 1969 Bill Regitz at Honeywell proposed 1C3T type DRAM cell with a source follower type MOS transistor output switch gate (VOG) . Intel hired Regitz with his 1C3T DRAM cell patent. Then in 1970 Intel introduced the 1101 DRAM chip which was the beginning to replace the magnetic digital core memory used in IBM main frame computers.



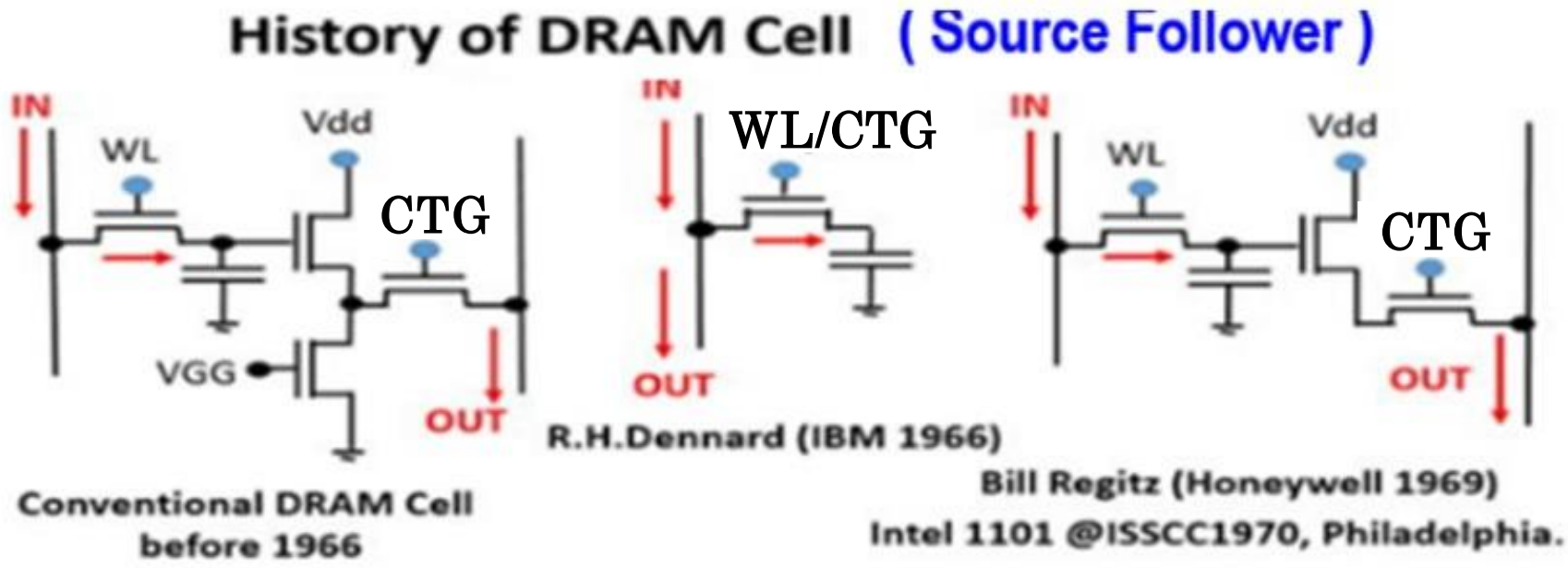
3 1T1C DRAM and Classical MOS type CTD

For 1C1T DRAM cell, the column sense amplifier circuit was needed for each column bit line to amplify the small signal charge in the large bit line read out capacitance.



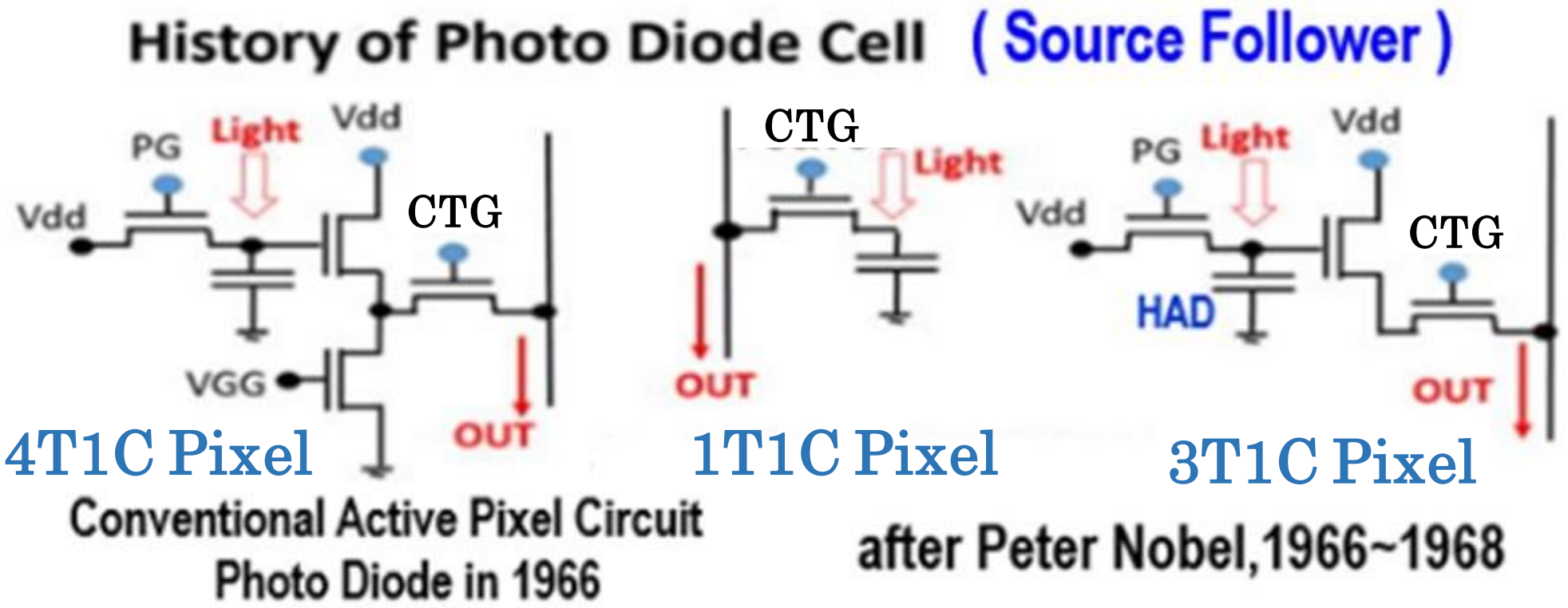
3 1T1C DRAM and Classical MOS type CTD

With the advancements of MOS process scaling technology and the circuit design technology, eventually the 1T1C DRAM cell became feasible for mass production.



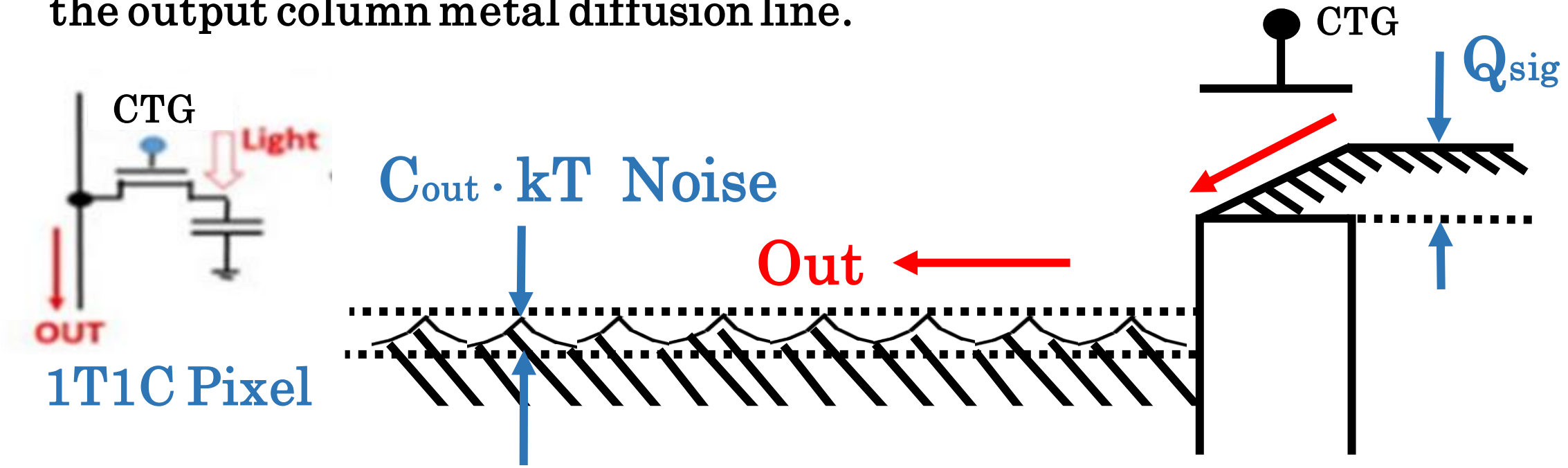
3 1T1C DRAM and Classical MOS type CTD

Independently from DRAM memory development efforts, conceptually the 4T1C and 3T1C active pixel MOS photo sensors were proposed by Peter Noble in 1968. But the 1T1C MOS image sensor was much simpler and feasible to mass production for consumer markets.



3 1T1C DRAM and Classical MOS type CTD

However the simple P+N single junction floating surface photodiode was used in the 1T1C MOS image sensor which has the serious image lag problem. Besides that, since the signal charge Qsig handled is a very small amount of analog nature, it is compatible to the (Cout)(kT) noise generated by random thermal (kT) movements of electrons in the output column metal diffusion line.



3 1T1C DRAM and Classical MOS type CTD

The thermal (Cout)(kT) noise is very similar to the ripple wave of the water surface of a lake which is a disturbance generated by a soft wind. Moreover the metal output signal column diffusion line has a very large capacitance Cout. The output signal level Vsig is very small, which is given by the relationship Vout = Qsig/Cout, and the picture quality of a simple MOS type CTD image sensor is expected very poor.